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Dynamic performance of H-bridge cascaded multilevel inverter with multiwinding transformer

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Abstract

This paper deals with minimization of the particular harmonics in the output voltage of inverter. The concept of multilevel voltage source inverters and their modulation topologies are to be analyzed. The concept of the Harmonic Stepped-Waveform with optimization technique for a multilevel inverter is to be presented. By applying this concept, specific harmonics can be eliminated, and the output voltage total harmonics distortion can be improved. A procedure to achieve the appropriate switching angles is to be proposed. This project also proposes an isolated cascaded multilevel inverter employing low-frequency three-phase transformers and a single dc input power source. The proposed circuit connection will reduce a number of transformers utilized when compared with traditional three-phase multilevel inverters.

Keywords: Harmonics, H-bridge cascaded multilevel inverter (HCMLI), Pulse Width Modulation, Total Harmonics Distortion, MATLAB

1. Introduction

Most of the multilevel inverters are having switches, capacitor voltage sources and can generate stepped output voltages with low harmonic distortions by controlling the switching devices properly. These multilevel inverters are broadly used in manufacturing factories and acquired public recognition as one of the new power converter fields because they can overcome the disadvantages of traditional Pulse Width-Modulation (PWM) inverters [5]. Multilevel inverters can be classified into diode clamped inverter, Flying capacitor inverter and cascaded H-bridge inverter with DC sources. The diode-clamped multilevel inverter needs complex PWM controls because more capacitors and diodes are necessary for generating output levels and adjusting the balance of each dc-link voltage of the capacitor [1]. Flying capacitor multilevel inverter circuit consists of relatively less elements. However, the volume of the system is enlarged for the necessity of more capacitors. In the case of the cascaded H-bridge-type multilevel inverter, each low-voltage H-bridge module has an independent dc-link voltage source [3,4]. The maximum number of output levels is only limited by isolation constraints. The merits are easy to control, flexibility and robustness. The demerit is that the independent dc-link voltage requires H-bridge separately [6]. To reduce the number of independent dc sources, replacing of reactors or capacitors method needs a minimum of three independent sources. Bidirectional switch method has been proposed to make sure the galvanic isolation between the input and output, but it has been observed that the circuit configuration is complex due to the use of bidirectional switches.

2. Working Principle of HCMLI

Consider a cascaded multilevel inverter with two H-bridges as shown in Fig.1 [2]. The H-bridge1 (H_1) is energized by a battery source of output voltage V_{dc}, while the H-bridge2 (H_2) is supplied by a capacitor whose voltage is to be held at V_C. That is, the capacitor acts as a DC source.
The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2 so that the output voltage of cascaded multilevel inverter [3] is

$$v(t) = v_1(t) + v_2(t)$$

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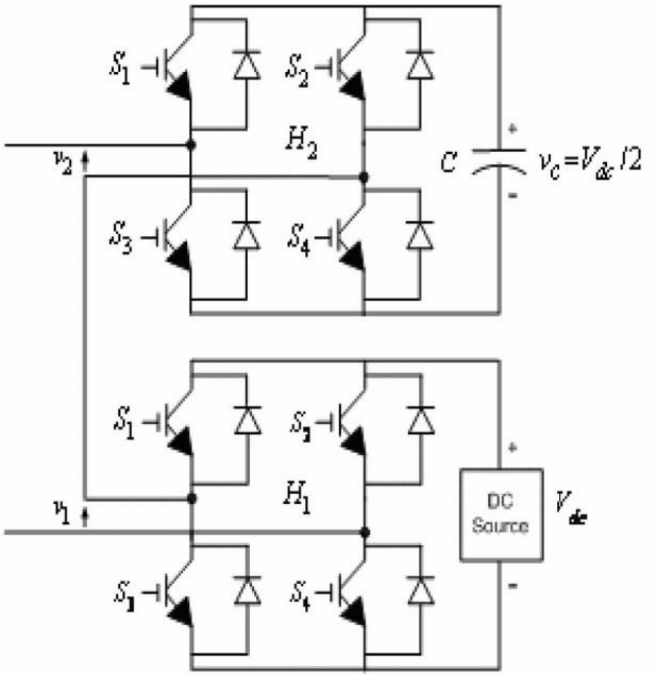

Figure1: Single-phase topology of multilevel inverter

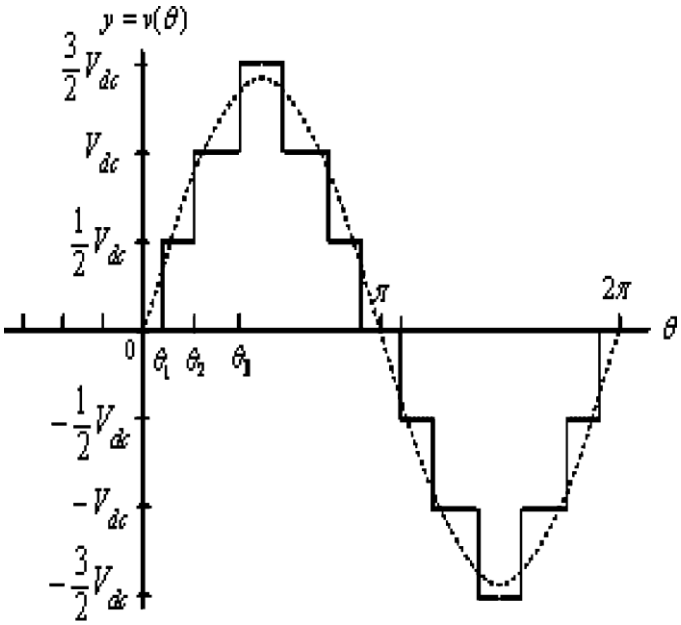

Figure 2: Seven-level equal step output-voltage waveform

By opening and closing the switches of H_1 properly, the output voltage v_1 can be made equal to $-V_{dc}$, 0 or V_{dc}, while similarly the output voltage of H_2 can be made equal to $-V_C$, 0 or V_C by opening and closing its switches appropriately. Therefore, the output voltage of the inverter can have the values $-(V_{dc} + V_C)$, $-V_{dc}$, $-(V_{dc} - V_C)$, $-V_C$, 0, V_C, $(V_{dc} - V_C)$, V_{dc} and $(V_{dc} + V_C)$ which constitute nine possible output levels.

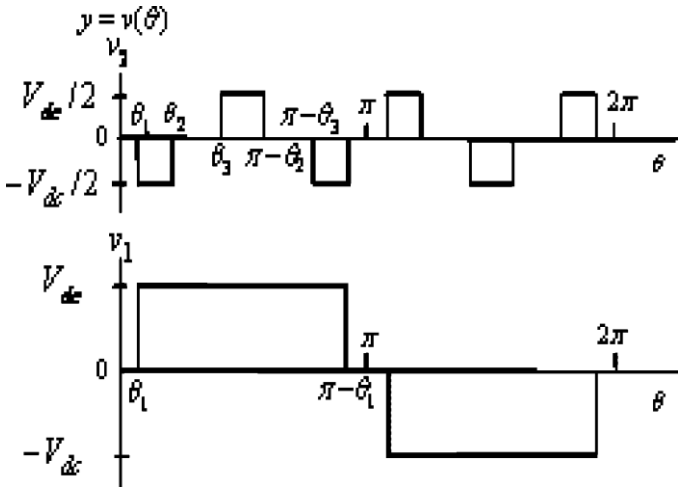

Figure 3: H-bridge voltages v_1 and v_2 control

A simple seven-level output voltage case $-3V_{dc}/2$, $-V_{dc}$, $-V_{dc}/2$, 0, $V_{dc}/2$, V_{dc}, $3V_{dc}/2$ can be designed as shown in Fig.2, when the capacitor's voltage V_C is chosen as $V_{dc}/2$. Table I shows how a waveform can be generated using the topology of Fig.1.

Table 1: Output voltages for a seven-level inverter

θ	v_1	v_2	$v = v_1 + v_2$
$0 \le \theta < \theta_1$	0	0	0
$\theta_1 \le \theta < \theta_2$	0	$V_{dc}/2$	$V_{dc}/2$
$\theta_1 \le \theta < \theta_2$	V_{dc}	$-V_{dc}/2$	$V_{dc}/2$
$\theta_2 \le \theta < \theta_3$	V_{dc}	0	V_{dc}
$\theta_1 \le \theta < л/2$	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$

Fig. 3 shows H-bridge voltages v_1 and v_2 control for $\theta_1 \le \theta < \theta_2$, $v_1 = V_{dc}$ and $v_2 = -V_{dc}/2$ and how the waveform of Fig.2 is generated if for $\theta_1 \le \theta < \theta_2$, $v_1 = V_{dc}$ and $v_2 = -V_{dc}/2$ are chosen.

3. Pulse Width Modulation Techniques

The main objective of the PWM is to control the output voltage of inverter and to decrease the harmonic content in the output voltage. The Pulse Width Modulation (PWM) techniques are generally used for voltage control. These techniques are most efficient and they control the drives of the switching devices. The block diagram of PWM technique is shown in figure 4.

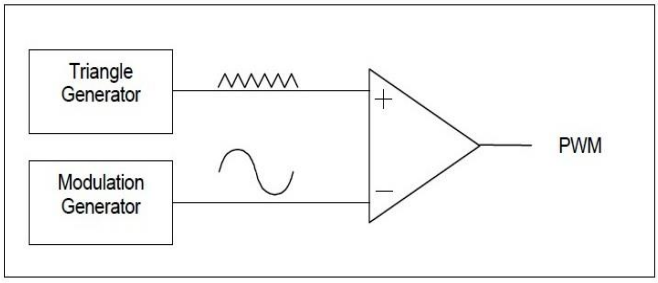

Figure 4: Block Diagram of PWM

The output voltage waveform is obtained by combining a triangle wave and a sine wave in which the triangular signal is the carrier/switching frequency of the inverter. The modulation generator makes a sine wave that determines the pulse width as well as the RMS voltage output of the inverter. However, several PWM switching patterns to eliminate harmonics in the output spectra of single-phase and three-phase inverters are possible. Each one of these alternatives leads to a specific advantage in single- and three phase inverters depending on the application. The superiority of the PWM techniques over the conventional carrier-modulated PWM's is established first. Next, a critical evaluation of the mentioned PWM schemes on the basis of application for single and three-phase inverters is provided, thereby providing the framework and guidelines for the selection of the appropriate technique for each application area. Evaluation criteria include harmonic loss factor and total harmonic distortion factors defined at the input and output of the inverter terminals. Finally, a simple low cost solution for obtaining the required PWM switching points is proposed. A PWM representation is shown in figure 5.

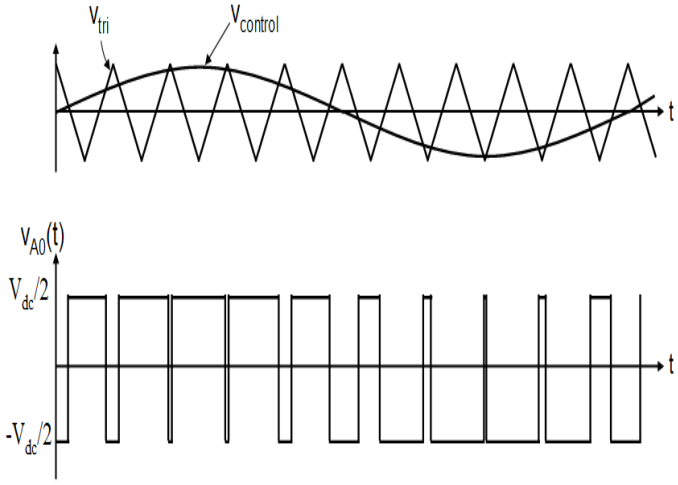

Figure 5: PWM representation

PWM schemes are widely classified as carrier-modulated sine PWM and pre-calculated programmed PWM schemes. Programmed PWM techniques are used to obtain high-performance results such as obtaining minimum losses, reduced torque pulsations, selective harmonic elimination, etc. It is interesting to note that the various objective functions chosen to generate a particular programmed PWM technique essentially constitutes the minimization of unwanted effects due to the harmonics present in the inverter output spectra. In view of this, little or no difference between each one of the programmed techniques is observed when significant numbers of low-order harmonics are eliminated. However, each one of the programmed PWM techniques is associated with the difficult task of computing specific PWM switching instants to optimize a particular objective function. This difficulty is encountered at lower-output frequency range due to a large number of switching instants.

4. Total Harmonic Distortion

Total Harmonic Distortion (THD) is a measurement of harmonic distortion present in a signal. It is defined as the ratio of sum of powers of all harmonic components to the power of fundamental frequency.

Harmonic contents are the major problem in power quality aspects in the power system network. Harmonics may be classified into voltage harmonics and current harmonics. Current harmonics are generated by harmonics in supply voltage which depends on the load. Both harmonics can be generated either by source or by the load. The sources are power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics may cause overheating of magnetic cores in electrical equipments [7]. On the other side, source harmonics are generated by non-sinusoidal voltage waveform. Voltage and current harmonics involve in power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives [8].

By applying Fourier transformation, the harmonic components can be extracted since any waveform must contain the superposition of fundamental and harmonic components. The frequency of each harmonic component is an integral multiple of its fundamental [9, 10]. There are several methods to indicate of the quantity of harmonics contents. The Total Harmonics Distortion (THD) which is defined in terms of the amplitudes of the harmonics Hn, at frequency nw0, where w0 is frequency of the fundamental component whose amplitude of H_1 and n is integer.

5. Proposed Cascaded H-Bridge Multilevel Inverter with Multiwinding Transformer

Fig. 6 shows a circuit configuration of the proposed multilevel inverter for three-phase applications [11, 12]. It consists of one single dc input source and several low-frequency three-phase transformers. By using the three-phase transformers, the number of transformers and the system volume may be reduced [13]. The transformer primary terminal is connected to an H-bridge module so as to produce V_{dc}, 0 and $-V_{dc}$. Every secondary of the transformer is connected in series to pile the output level up. Moreover, each phase terminal is delta connected to restrain the third harmonic component.

Fig. 7 shows a predigested representation of Fig. 6 when it employs three three-phase transformers. As shown in Fig. 7, the primary of each transformer is a three-phase one, and each secondary is a single-phase terminal. Three terminal outputs are series connected to generate the voltage V_{AS}. In this arrangement, each phase can be expressed independently and called as isolated H-bridge cascaded multilevel inverter [14]. In Fig. 6, V_{ak}, V_{bk} and V_{ck} mean the output voltages of the H-bridge inverter connected to the k^{th} transformer. Here, V_{Ak}, V_{Bk} and V_{Ck} are the output voltages of the transformers in each phase.

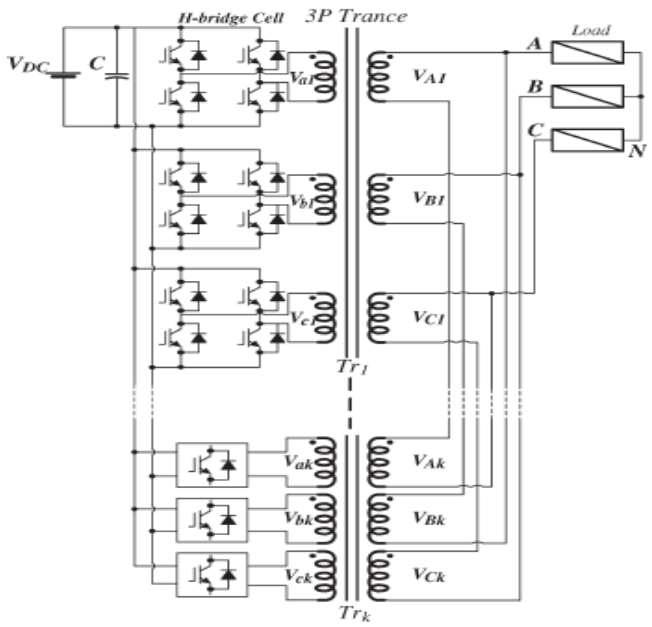

Figure 6: Circuit configuration of the proposed multilevel inverter

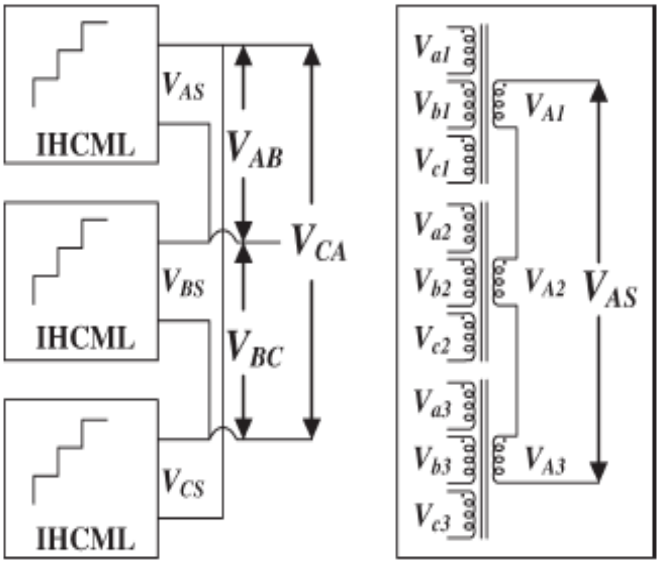

Figure 7: Simplified structure of the proposed multilevel inverter

6. Simulation of H-Bridge Cascaded Multilevel Inverter

Fig. 8 shows Simulation model of three phase CMLI. This model consists of three subsystems. Each subsystem block contains the seven level CMLI. The voltage measurement of the each subsystem is done by voltage measurement block. The output reduced harmonics waveform is shown by the scope block. The scope block displays its input with respect to simulation time. The Scope block can have multiple axes (one per port); all axes have a common time range with independent y-axis. In our project we use the x–axis parameter as time in seconds and the y–axis parameter is phase voltage.

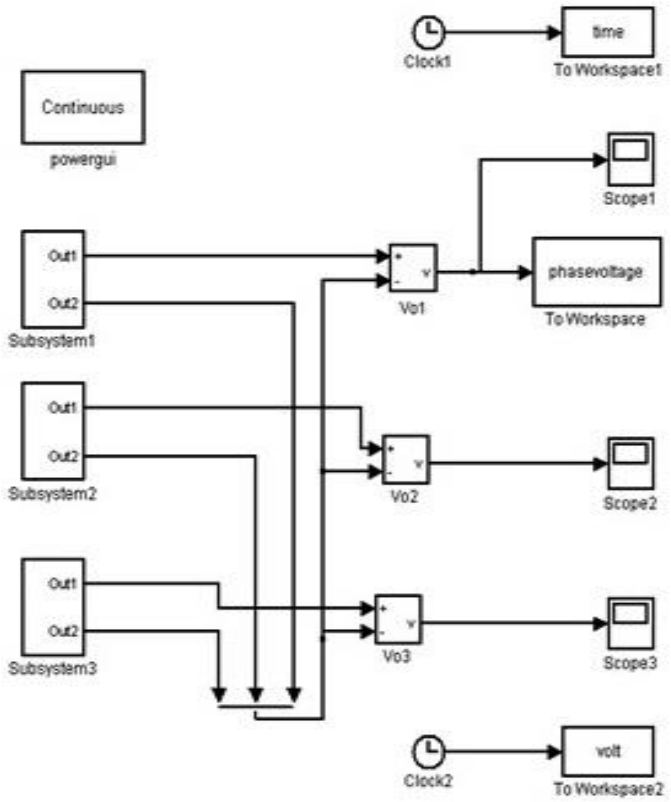

Figure 8: Simulation model of three phase HCMLI

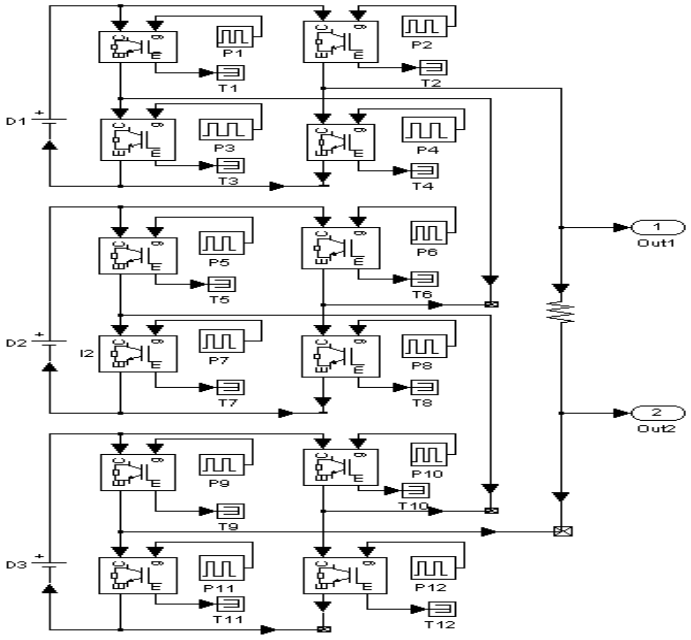

Figure 9: Subsystem model of HCMLI

The figure 9 shows the HCMLI model for the first subsystem. The Pulse Generator block generates square wave pulses at regular intervals. The shape of the generated waveform depends on the parameters, Amplitude, Pulse Width, Period,

and Phase Delay. The terminator block is used to limit blocks for avoiding warning messages whose output ports are not connected to other blocks. The pulse duration for switches S1, S2, S3 and S4 is 83.4%. The pulse duration for switches S5, S6, S7 and S8 is 66.6%. The pulse duration for switches S9, S10, S11 and S12 is 41.7%.The Fig. 10 shows the Output Wave form of H-Bridge Multilevel Inverter. The figure 11 shows the Harmonic profile of the H-Bridge Cascaded Multilevel Inverter. From the harmonic profile results, it can be observed that the Total Harmonic Distortion around 10.55% only. The third order harmonics magnitude is only 2.8% and fifth order harmonics is 2.9%.

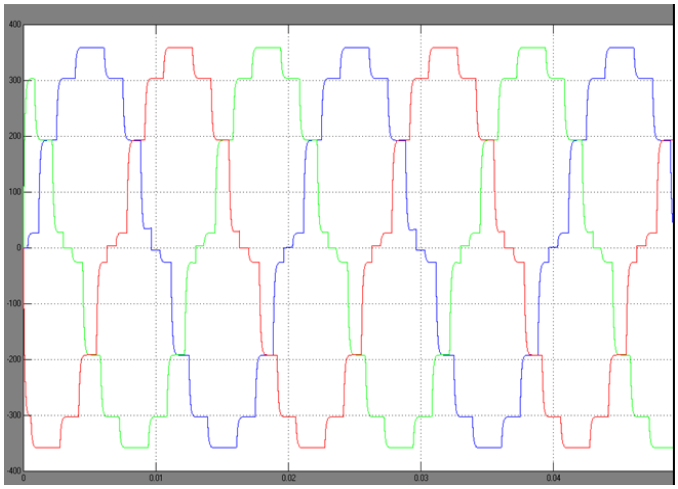

Figure 10: Output Wave form of H-Bridge Cascaded Multilevel Inverter

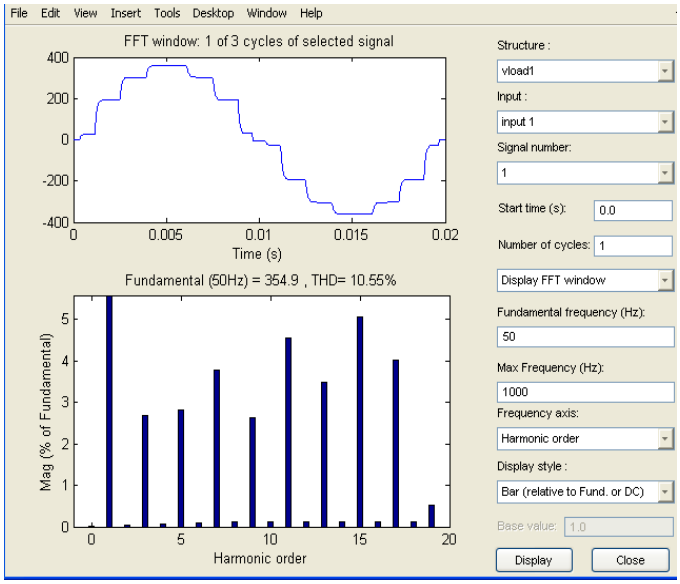

Figure 11: Harmonic profile of the H-Bridge Cascaded Multilevel Inverter

7. Conclusion

The disturbances in power electronics equipment are often periodic and rich in higher harmonics. They have known frequencies and are often above the bandwidth of regulators used to control fundamental components. Therefore, the "regular" control can only partially reduce their effects on the distortion of control variables. The hybrid cascaded multilevel inverter uses only one power source for each phase while producing desired multilevel voltage waveforms. Cascaded multilevel inverter has been simulated using MATLAB. The output voltage of simulated three phase HCMLI and the harmonic profile are obtained. From the harmonic profile results, it can be shown that the THD is around 10.55% only. The third order harmonics magnitude is only 2.8% and fifth order harmonics is 2.9% only.

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