



RESEARCH PAPER

Deep-Cryogenic Performance and Reliability Analysis of High-k Stacked Dual-Gate Junctionless MOSFETs for Advanced CMOS and RF Applications

Nidhi, Amrita Pahadia

Department of Electronics and Communication Engineering (VLSI Design), Lakshmi Narain College of Technology (LNCT), Bhopal, India

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Abstract

As many new quantum-classical electronic devices are developed, the performance and reliability of nanoscale transistors at very low temperatures are now another critical consideration. This paper thoroughly explores stacked dual-gated junctionless transistors with a high-k device structure in the deep sub-cryogenic regime down to 50 K. The study is conducted to provide a complete characterization of the device behavior, including DC, analog, and radio-frequency (RF) characterization. The important electrical attributes, such as subthreshold swing, transfer behavior, ON current, OFF leakage current, transconductance, and the RF figure of merit, are analysed and discussed, including their temperature dependence. These interface-trap charge densities (η_{itc}) are also studied to assess their impact on device characteristics and to determine reliability under actual operating conditions. The simulations show gains in Electrostatic Control (EC) in the channel when the operating temperature is reduced. The gains include better switching behavior, lower leakage current, and sharper sub-threshold slope. There is also an increase in carrier transport at cryogenic temperatures, which improves analog performance and RF characteristics, making the proposed architecture suitable for low-temperature applications. The outcomes presented here suggest that a high-k stacked DG junctionless MOSFET can also be a candidate for future (cryogenic) CMOS platforms. This device architecture is attractive for low-power, high-speed, reliable electronic systems. It is suitable for integration into next-generation quantum computing and advanced cryogenic signal-processing applications.

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1. Introduction

The evolution of the modern integrated circuit has mainly resulted from continuous scaling. This scaling of CMOS technology is the key factor for advancing modern integrated circuits. Following Moore's law, the semiconductor industry has been shrinking transistor sizes to make devices more compact, faster, and more power-efficient for years [1, 2]. Scaling down the gate lengths, however, poses various difficulties, such as increased leakage current, short-channel effects (SCEs), increased static power dissipation, threshold voltage degradation, and complex junction formation at the source and drain. These restrictions have a significant impact

on the performance, reliability, and scalability of conventional MOSFET architectures, especially at the nanoscale. One of these is the junctionless field-effect transistor (JLFET), which I described in Joubert et al. [3] and is a promising candidate for future nanoelectronics applications. One of the differences between the junctionless and conventional MOSFETs is that the junctionless device has a uniformly doped channel that is continuous without any abrupt junction. This is a novel design that makes fabrication easier, reduces manufacturing complexity, and reduces short-channel degradation mechanisms. Additionally, there is less process variety, and device scalability is lower due to missing junction engineering. Another viable way to improve overall and/or individual

Corresponding author: Nidhi

Email Address: nidhikuhla@gmail.com

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device performance is through so-called gate dielectric engineering. HfO_2 has been extensively studied because it is a material with a large dielectric constant, good thermal stability, and suitability for integration into existing CMOS fabrication technologies. The addition of a thin silicon dioxide (SiO_2) interfacial layer and the same gate metal to create a stacked gate dielectric structure is beneficial both for electrostatic integrity and for reducing OFF-state leakage current (I_{OFF}) [4]. Consequently, high-k stacked, DG, junctionless MOSFETs are a promising device for low-power, high-performance electronic systems. Recent advances in quantum computing technologies create new opportunities and challenges for semiconductor device design. The computational advantages of quantum processors have been demonstrated in certain domains of application, and the area of hybrid classical-quantum computing infrastructure is becoming a very active research field [5, 6]. Operating at ultra-low temperatures is certainly one of the most crucial requirements for many quantum systems, in which the qubit can achieve a long coherence time and perform well-defined quantum operations reliably. For many of these operations, the qubits will be "cold," with temperatures typically well below 10 K to enable qubit manipulation, readout of the information stored in the qubits, and error correction. The use of these cryogenic CMOS platforms could open the way to compact, scalable quantum processors capable of supporting large-scale computation [8-10]. Low-temperature investigations of semiconductor devices are not new. Applications such as space exploration systems, scientific instrumentation, and aerospace electronics have been widely explored for MOS-based technologies at LNT (≈ 77 K) over the past few decades [11]. However, with the advent of quantum technologies and the complexity of modern electronic systems, there's been renewed interest in understanding devices under temperatures below the established liquid nitrogen range. Reduced supply-voltage operation and timing requirements in quantum circuits fabricated with CMOS technology have been highlighted in previous studies [12,13]. The magnitude of several important transistor parameters is significantly affected by temperature changes. Operating temperature (OT) is seen to have a significant effect on electrical characteristics like ON-state current (I_{ON}), I_{OFF} , subthreshold slope (SS), carrier transport dynamics, transconductance, voltage transfer characteristics (VTC), noise margins, and energy band profile [14]. In the low-temperature regime, phonon scattering is greatly suppressed, thereby improving carrier mobility and further enhancing transport efficiency. Simultaneously, the device's electrostatic behavior changes due to impurity freeze-out and carrier concentration effects. Therefore, the low-temperature behavior of heretofore described typically exhibits better switching performance, lower leakage currents, and better current drive performance. The ON/OFF current ratio ($I_{\text{ON}}/I_{\text{OFF}}$) and the subthreshold swing are among the various performance indicators that are more sensitive towards the cryogenic operation. This is because both parameters are temperature-dependent, and the lower the OT, the steeper the switching characteristics, resulting in a very significant decrease in standby power consumption [15]. This would be very beneficial for ultra-low-power electronic circuits and quantum computer interfaces.

However, it is also important to note that at very low temperatures, operation exhibits characteristic physical phenomena that cannot be described using the views and models of room-temperature operation. Theoretically, lower temperatures will lead to better SS, but experiments have shown that the true 'saturation value' of SS is close to 10 mV/dec at deep cryogenic (DC) operation [16–19]. This may point to weaknesses in the classical Boltzmann approach and the necessity of device-level analysis under cryogenic conditions. Keeping this in mind, the current study aims to explore the static, analog, and radio-frequency (RF) characteristics of a stacked Dual-Gate Junctionless MOSFET in DC conditions. A comprehensive list of performance metrics is used to investigate the proposed device – known as the DCT-DG-JL-MOSFET systematically. Important analog parameters, such as transconductance (g_m) and transconductance generation factor (g_m/I_{ON}), along with important RF figure of merits, such as parasitic capacitances, cut-off frequency (f_T), Gain-Bandwidth product (G_{BW}), Unilateral power gain, and Stern stability factor (K_{stable}), are analysed. In addition, the effect of interface-trap charge density (η_{itc}) on the device's transfer characteristics and transconductance at low temperature is investigated for device reliability. This practical study examines the potential application of the proposed transistor structure in future cryogenic CMOS and quantum computers.

2. Device Architecture and Simulation Set-up

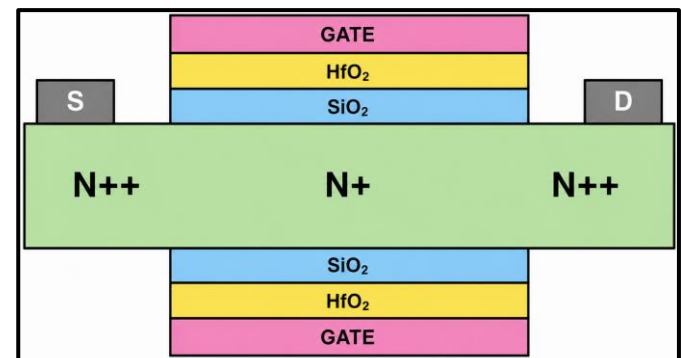


Figure 1: Schematic cross-sectional view of the proposed high-k stacked DG junctionless MOSFET (DCT-DG-JL-MOSFET).

Fig. 1 shows the schematic structure of the proposed Dual-Gate Junctionless MOSFET (DG-JL-MOSFET) working under the DC condition. The device has a uniformly doped N-channel sandwiched between heavily doped source and drain regions. On both sides of the channel, a stacked gate dielectric of HfO_2 and SiO_2 is used to improve electrostatic control, reduce leakage current, and enhance device operation in the cryogenic regime. To achieve equal carrier transport and eliminate the abrupt junction, a constant doping concentration of (10^{18} cm^{-3}) is used over the channel region. A stacked gate dielectric structure is employed to provide excellent electrostatic control with a minimal leakage current. The stack is a high-k hafnium dioxide (HfO_2) layer followed by a low-k silicon dioxide (SiO_2) layer. The thicknesses of HfO_2 and SiO_2 layers are fixed to 2 nm and 1 nm, respectively. The optimum combination of

dielectric materials has been found to yield good gate coupling and low ON-state leakage. The silicon body thickness has been manually adjusted to 10 nm to ensure optimum control of the charge distribution in the channel. Further, a metal with a work function of 4.8 eV has been employed as the gate electrode, demonstrating the voltage characteristics and stability desired in the device. The proposed structure is characterized by its Electrical and Electronic properties, as modeled using the SILVACO ATLAS Technology Computer-Aided Design (TCAD) platform [20]. Thermal effects have been added to the GIGA self-heating simulation framework, which has been run in the ATLAS environment to capture their impact at cryogenic temperatures accurately. The LAT is a model of the lattice's temperature distribution. The HEAT was a collection of heat-suit caps. The FULL model is selected to account for thermal generation/heat transfer phenomena in the device. To obtain solutions to the heat-flow equations and to identify thermal equilibrium during simulation, appropriate thermocontact boundary conditions are also used. The drift-diffusion formalism is used to describe carrier transport in the channel, balancing computational accuracy with simulation complexity. In nanoscale devices, recombination mechanisms such as Shockley-Read-Hall (SRH) become significant, so this recombination is incorporated into the simulation framework. The analytic mobility model accounts for variable mobility as a function of temperature. This model provides a good approximation of the effect of cryogenic operation on carrier transport. Mutations in these physical devices can enable realistic modelling of device behavior across a broad temperature range.

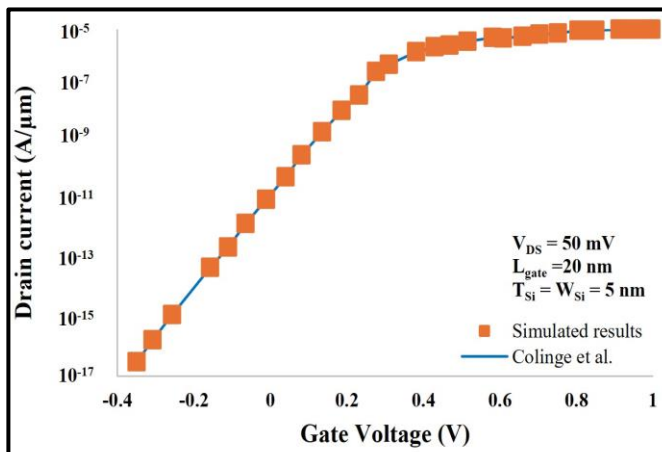


Figure 2: Validation of the TCAD simulation model through comparison of simulated transfer characteristics with the experimental results reported by Colinge *et al.* [3].

Fig. 2 presents the validation of the proposed TCAD simulation framework by comparing the simulated transfer characteristics of the junctionless MOSFET with the experimental results reported by Colinge *et al.* [3]. The drain current (I_D) variation with gate voltage (V_g) demonstrates excellent agreement between the simulated and measured data over the entire operating range. The high degree of matching between the two characteristics confirms the correctness of the physical models and the simulation parameters used in this

study. This validation will confirm the validity of the SILVACO ATLAS TCAD methodology for investigating the electrostatic, analog, RF, and reliability performance of the proposed DCT-DG-JL-MOSFET.

Although significant advancements have been made in cryogenic CMOS technologies, a comprehensive investigation of high-k stacked DG junctionless MOSFETs operating in the DC regime remains limited. The analog performance, RF stability, interface-trap reliability, and transient behavior have generally been studied less than the DC characteristics, with less attention given to combining these attributes in a single assessment. In addition, to the best of our knowledge, the effect of polarized η_{itc} on the electrostatic and analog performance of DG junctionless devices at DCTs has yet to be well studied. Hence, in this work, a detailed analysis of a high-k stacked DG Junctionless MOSFET for the complete temperature range from 400K to 50K has been presented. This study delves deeper into DC, analog, and RF performance; analyzes device stability using the Sattel effect stability factor; assesses the effect of interface-trap charges on device reliability; and examines transient response characteristics for future cryogenic CMOS and quantum computing applications. The major contributions of this work are summarized as follows:

- Investigation of a high-k stacked DG junctionless MOSFET under DCTs ranging from 400 K to 50 K.
- Comprehensive evaluation of analog, DC, and RF performance metrics, including transconductance, transconductance generation factor, gain-bandwidth product, cut-off frequency, and unilateral power gain.
- Reliability assessment through interface trap charge density analysis under positive and negative trap conditions.
- RF stability investigation using the Stern stability factor for cryogenic operation.
- Analysis of transient switching behavior and settling-time characteristics for high-speed cryogenic electronic applications.

3. Simulation Outputs

3.1 Impact of DCT on the DC Metrics

The extension of the deep-cryogenic operation window for the proposed DCT-DG-JL-MOSFET, from 400 K to 50 K, was analysed to assess the impact of DC operation on the transistor's electrostatic and switching characteristics. In nanoscale devices operating under cryogenic conditions, temperature changes significantly affect carrier transport mechanisms. The phonon scattering is reduced at low temperatures; therefore, the charge transport is modified by the different behavior of the charge carriers due to the reduced effectiveness of impurity ionization. Moreover, at extremely low temperatures, carrier mobility is affected by additional scattering mechanisms, in addition to lattice scattering, such as Coulombic interactions and surface scattering [21].

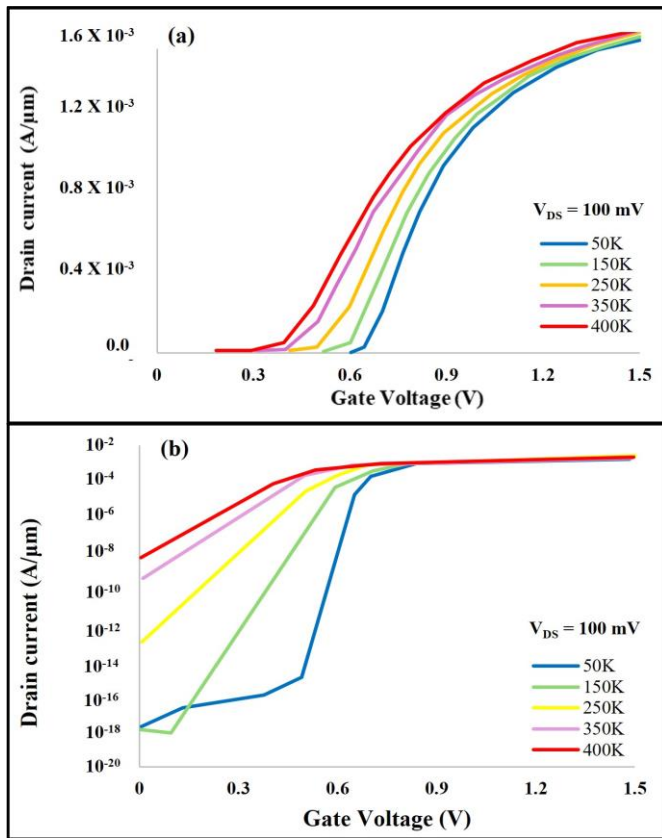


Figure 3: Transfer characteristics of the proposed DCT-DG-JL-MOSFET at different temperatures: (a) linear-scale I_{DS} - V_{GS} characteristics and (b) logarithmic-scale I_{DS} - V_{GS} characteristics.

Fig. 3 illustrates the transfer characteristics (I_{DS} - V_{GS}) at OTs from 50K to 400K with $V_{DS}=100$ mV. Fig. 3(a) demonstrates the linear-scale characteristics, whereas Fig. 3(b) depicts the corresponding logarithmic response. There is a significant temperature-dependent change in the transfer curves as the temperature is reduced from 400 K to 50 K, revealing a strong temperature dependence in the device's electrostatic behavior. The efficiency of the cryogenic operation provides better channel control and fewer thermally generated carriers, resulting in a significant decrease in leakage current. In addition, the log bistable shape provides better switching characteristics at lower temperatures due to lower ON-to-OFF current and steeper subthreshold conduction. Experimental temperature variation demonstrates that the proposed High-K stacked DG Junctionless MOSFET exhibits better electrostatic integrity and good low-power performance at DCTs.

The surface potential distribution along the channel of the designed DCT-DG-JL-MOSFET is demonstrated in Fig. 4 for various OTs ranging from 50K to 400K. The device shows enhanced electrostatic control of the channel as the temperature decreases, thereby yielding a better potential profile. The increased gate control for devices under DC conditions reduces leakage conduction, increases channel modulation, and improves switching performance, thereby demonstrating the proposed device's suitability for applications such as low-power cryogenic CMOS devices.

The ON/OFF current ratio (I_{ON}/I_{OFF}) of the proposed DCT-DG-JL-MOSFET over the OT range of 50 K to 400 K is shown in

Fig. 5 for $V_{DS} = 100$ mV. As the OT is reduced, a progressive rise in switching ratio was observed, indicating Electrostatic control in a DC environment. There is efficient current conduction in the ON state, and the strong gate-channel coupling effectively suppresses the OFF-state leakage current. As a result, the I_{ON}/I_{OFF} ratio is much larger at lower temperatures, enabling higher switching efficiency and reduced static power dissipation. The features indicate that the proposed high-k stacked dual-gate junctionless MOSFET can be used in low-power cryogenic CMOS circuits and quantum computing applications that require reliable operation and low power consumption.

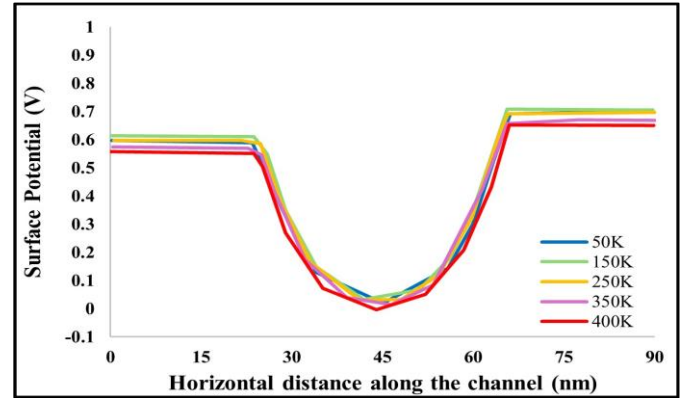


Figure 4: Surface potential distribution along the channel of the proposed DCT-DG-JL-MOSFET at different operating temperatures.

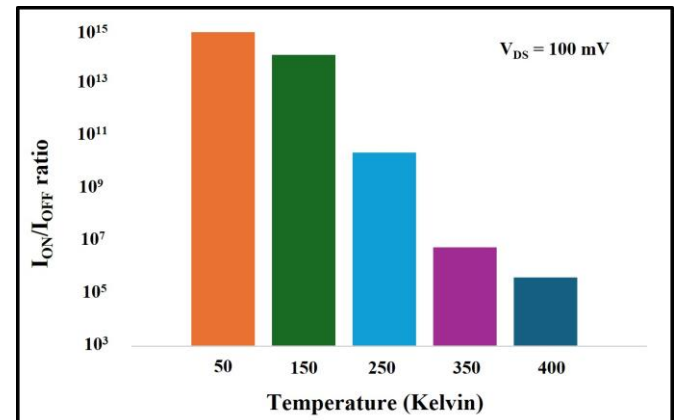


Figure 5: Variation of the ON/OFF current ratio (I_{ON}/I_{OFF}) of the proposed DCT-DG-JL-MOSFET at different operating temperatures.

Fig. 6 demonstrates the change in subthreshold slope (SS) with temperature for the proposed DCT-DG-JL-MOSFET over the range 50K-400K. It is observed that at higher temperatures, the SS shows an increasing trend, whereas the minimum value is obtained under DC conditions. The lower SS at the reduced temperatures indicates tighter control of the gates over the channel, meaning quicker switching between the OFF and ON states with less change in χV -gates. Thus, the device shows higher switching efficiency, lower subthreshold leakage, and improved electrostatic performance. Improved subthreshold performance at cryogenic temperatures also encourages the use in low-power CMOS and quantum computers.

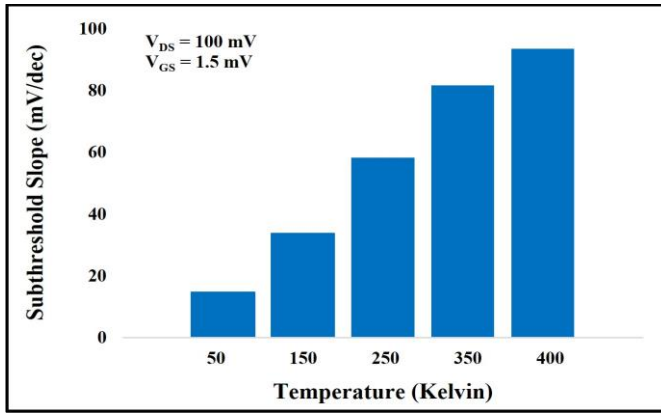


Figure 6: Variation of the SS of the proposed DCT-DG-JL-MOSFET at different operating temperatures.

The relation of temperature dependence of SS can be given as Eq. (1) [22]:

$$SS = \frac{\gamma K_{\text{Boltzmann}} T}{e} (\ln 10) \quad (1)$$

The subscript e denotes the electronic charge, γ is the subthreshold slope factor, and $K_{\text{Boltzmann}}$ is the Boltzmann constant. This is as anticipated by Eq. (1); the sub-threshold slope decreases monotonically with decreasing temperature, resulting in increased switching behavior. The best gate control and highest switching efficiency occur at the minimum SS value of 50 K. This is useful for low-voltage and cryogenic electronic circuits and will be important for future electronic applications, particularly quantum computing, which will require energy-efficient operation. The electrostatic performance of the proposed DCT-DG-JL-MOSFET is significantly improved at 50 K compared to that at 400 K. Overall, the various SNM reduction mechanisms and the associated static power reduction and improvements in ON/OFF current ratio are benefits of operating under cryogenic conditions, enhancing switching characteristics and reducing leakage current.

3.2 Impact of DCT on the Analog Metrics

The g_m characteristics of the proposed DCT-DG-JL-MOSFET are shown in Fig. 7 for V_{DS} of 100 mV in the following OTs: 50 K, 100 K, 150 K, 200 K, 273 K, 300 K, 350 K and 400 K. Initially, an increasing transconductance with the V_g results from the progressive channel formation and improved carrier movement, up to a maximum, and then falls slightly with higher gate biases. This is due to mobility degradation induced by increased carrier scattering and the magnitude of lateral electric fields within the channel.

The effective working temperature computed at 50 K yields the highest transconductance, highlighting the advantages of DC operation for carrier mobility. Transconductance maximum values increase as temperature rises from 50 K to 400 K, and the peak values shift to lower V_g . It is also found that transport efficiency decreases. The enhanced g_m observed at cryogenic temperatures confirms the superior analog performance of the proposed device, making it well suited for low-power analog

and mixed-signal circuit applications. This is similar to what was observed in other nanoscale MOSFET investigations [23, 24]. The effect of temperature on transconductance is quite apparent from the characteristics plotted. As a result, minority-carrier mobility and transport efficiency increase at lower temperatures, leading to higher mobility and efficiency in the silicon lattice. Thus, higher transconductance is obtained during cryogenic operation. A sharp rise in the analog with decreasing temperature is observed at 50 K, while a gradual decrease in (g_m) is observed with increasing temperature towards 400 K. The improved transconductance at the low temperatures used in the experiments is mainly due to impurity binding and low-lattice-scattering mechanisms that enhance carrier transport along the channel [37, 38].

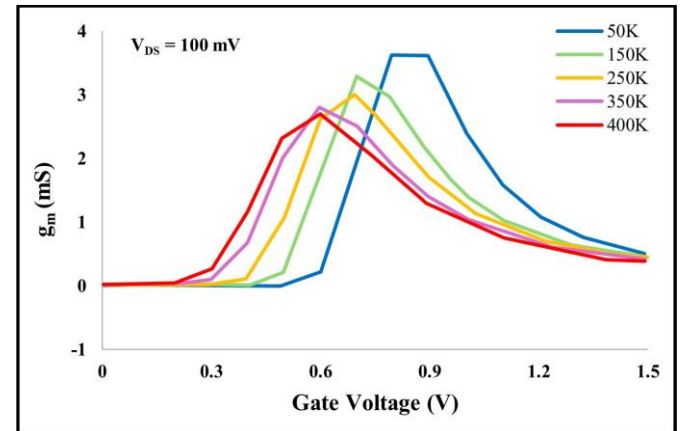


Figure 7: Transconductance (g_m) characteristics of the proposed DCT-DG-JL-MOSFET at different OTs ($V_{DS}=100$ mV).

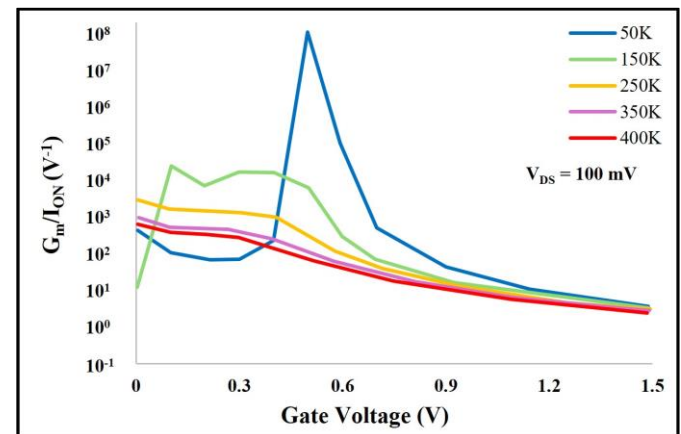


Figure 8: Transconductance generation factor (g_m/I_{ON}) characteristics of the proposed DCT-DG-JL-MOSFET at different OTs ($V_{DS}=100$ mV).

Fig. 8 illustrates the g_m/I_{ON} of the proposed DCT-DG-JL-MOSFET at OTs from 50 K to 400 K with $V_{DS}=100$ mV. The g_m/I_{ON} ratio serves as an important figure of merit for evaluating the transconductance efficiency of analog and RF devices. As shown in the figure, the proposed device exhibits the highest g_m/I_{ON} values under DC operation, indicating improved transconductance efficiency with lower current consumption. The g_m/I_{ON} characteristics gradually decrease with increasing temperature from 50K to 400K due to reduced

carrier mobility and increased scattering. Since g_m/I_{ON} is inversely related to the subthreshold slope, the improved values at cryogenic temperatures demonstrate superior energy efficiency, making the proposed device highly suitable for low-power analog and RF applications [20].

3.3 Impact of DCT on RF Metrics

Fig. 9 presents the variation of the intrinsic parasitic capacitances of the proposed DCT-DG-JL-MOSFET at OTs from 50K to 400 K. Fig. 9(a), Fig. 9(b), and Fig. 9(c) demonstrate the (C_{gs}), (C_{gd}), and (C_{gg}), respectively. At lower V_g , all capacitances remain nearly constant because the device operates in the weak inversion region with limited channel charge. As the V_g increases, a sharp rise in capacitance is observed due to channel inversion and enhanced carrier accumulation beneath the gate.

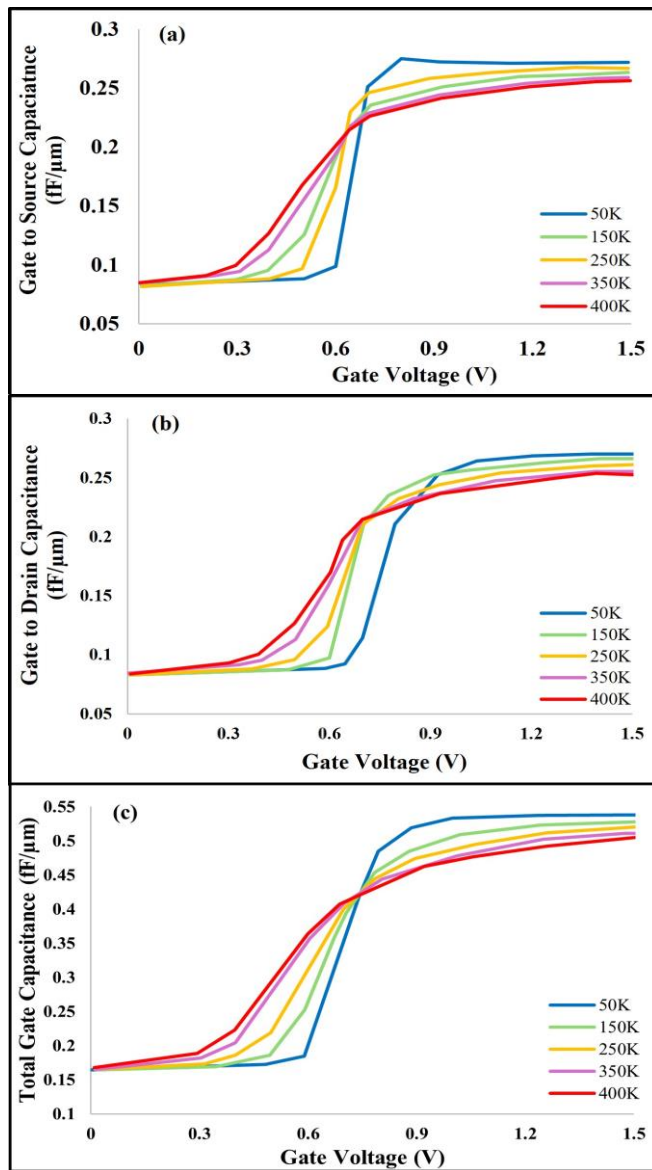


Figure 9: Variation of intrinsic parasitic capacitances of the proposed DCT-DG-JL-MOSFET at different operating temperatures: (a) C_{gs} , (b) C_{gd} , and (c) C_{gg} .

The maximum capacitance values are obtained at 50 K, indicating stronger gate control and improved channel charge modulation under DC conditions. The temperature-dependent capacitance characteristics demonstrate that cryogenic operation enhances electrostatic coupling and supports superior high-frequency performance, making the proposed device suitable for RF and high-speed cryogenic electronic applications. The strongest gate control and higher charge coupling under cryogenic conditions are seen for temperatures of 50 K among those investigated, which corresponds to the highest capacitances [26,27]. The weak inversion region yields lower capacitance values. Thermally generated carriers are reduced at DCTs, thereby altering the threshold voltage, channel charge distribution, and capacitance characteristics [21,28]. Therefore, the gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and total gate capacitance (C_{gg}) temperature dependence directly impacts all RF aspects of the device. The frequency ($F_{transit}$) parameter is computed using Eq. (2) as follows [29,30]:

$$F_{transit} = \frac{g_m}{2\pi(C_{gg})} \quad (2)$$

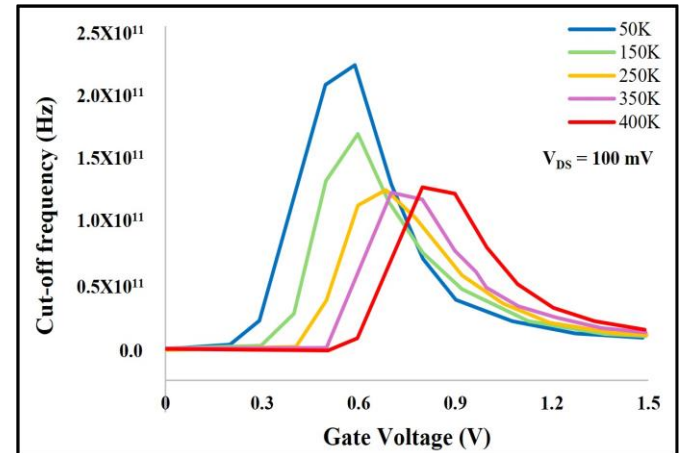


Figure 10: Cut-off frequency (f_T) characteristics of the proposed DCT-DG-JL-MOSFET at different OTs ($V_{DS}=100$ mV).

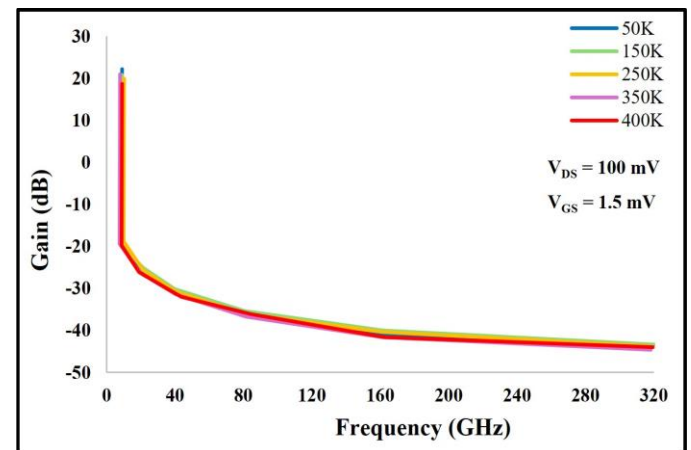


Figure 11: Unilateral power gain (U_{gain}) characteristics of the proposed DCT-DG-JL-MOSFET at different operating temperatures.

Fig. 10 illustrates the cut-off frequency (f_T) characteristics at OTs from 50 K to 400 K with $V_{DS}=100$ mV. The f_T increases rapidly with V_g , reaches a maximum value, and then gradually decreases at higher gate biases. The highest f_T is obtained at 50 K, owing to enhanced carrier mobility, higher transconductance, and improved electrostatic control under DC conditions. The exact cut-off frequency has been observed to decrease with increasing OT due to reduced carrier transport efficiency and increased scattering. The results demonstrate that the proposed device can operate at high frequencies in a cryogenic regime, making it suitable for RF and quantum CMOS applications.

The unilateral power gain, or U_{gain} , of the proposed DCT-DG-JL-MOSFET at various OTs (50 K - 400 K) for $V_{DS}=100$ mV and $V_{GS}=1.5$ mV is demonstrated in Fig. 11. For all temperature levels, the gain decreases with increasing operating frequency. It is observed that the shoot-through of the sheath currents can be enhanced under DC operation, with a comparatively higher gain at 50 K, indicating improved RF amplification capability, higher carrier mobility, and stronger electrostatic control. The 0 dB gain frequency corresponds to the maximum oscillation capability of the device, an important measure of the device's RF performance and amplifier stability [31]. The outputs confirm the compatibility of the proposed DCT-DG-JL-MOSFET for use in high-frequency cryogenic RF applications.

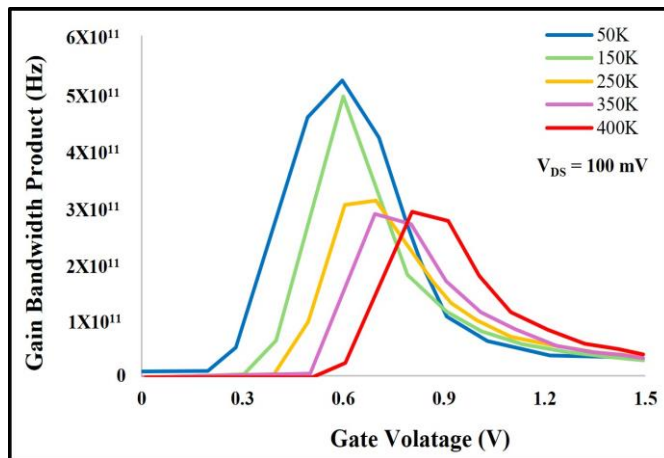


Figure 12: Gain-bandwidth product (G_{BW}) characteristics of the proposed DCT-DG-JL-MOSFET at different OTs ($V_{DS}=100$ mV).

The GBW product of the proposed DCT-DG-JL-MOSFET at various OTs ranging from 50 K to 400 K is demonstrated in Fig. 12 for $V_{DS} = 100$ mV. As the V_g increases, the GBW rises to a maximum in the moderate inversion region, then falls as the V_g is further increased. This is because electrostatic control, transconductance, and carrier mobility are better at 50 K, which maximizes the GBW. These results demonstrate that DC operation yields an excellent frequency response and bandwidth for the proposed device in high-speed analog and RF applications.

$$G_{BW} = \frac{g_m}{2\pi 10(C_{gd})} \quad (3)$$

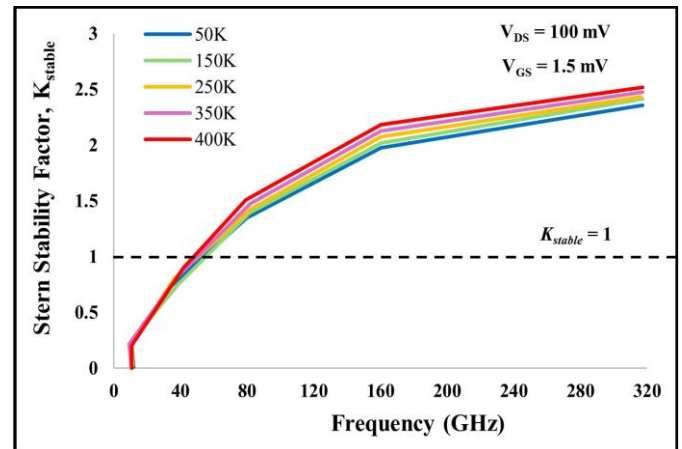


Figure 13: Stern stability factor (K_{stable}) characteristics of the proposed DCT-DG-JL-MOSFET at different OTs, demonstrating unconditional RF stability over a wide frequency range.

The Stern stability factor (K_{stable}) of the proposed DCT-DG-JL-MOSFET is demonstrated as a function of operating frequencies at 50 K, 150 K, 250 K, 350 K, and 400 K with a $V_{GS} = 1.5$ mV and a $V_{DS} = 100$ mV, as demonstrated in Fig. 13. The small-signal Y-parameters are used to obtain the Stern stability factor that is used in a wide range of applications for assessing the unconditional stability of RF transistors and amplifier circuits [31]. For all temperatures, K_{stable} increases with increasing operating frequency. The dash-marked reference line at $K_{stable} = 1$ is the stability criterion, with values exceeding unity representing unconditional stability. As shown in the figure, the proposed device operates stably with $K_{stable} > 1$ for temperatures ranging from 298 K to 673 K and up to about 50 GHz, indicating stable operation over a broad RF frequency range. In addition, DC operation is beneficial for RF stability, owing to improvements in carrier transport properties, electrostatic control, and scattering effects. The enhanced stability at low temperatures will establish the proposed DCT-DG-JL-MOSFET as a potential candidate for high-frequency cryogenic CMOS circuits, low-noise RF amplifiers, and quantum computing interface circuits requiring stable, robust operation at low temperatures [32,33].

3.4 Impact of DCT on Interface Trap Charges

Nanoscale MOSFETs are greatly influenced by the presence of η_{itc} at the semiconductor–dielectric interface, which greatly affect the reliability and long-term stability of nanoscale MOSFETs. The defect states are normally created during fabrication and device processing and serve as recombination-generation centers, which have a significant influence on carrier transport and the device's electrostatic behavior, via the Shockley–Read–Hall (SRH) mechanism [34]. Fig. 14 demonstrates the influence of η_{itc} on the transfer characteristics of the proposed DCT-DG-JL-MOSFET for trap densities varying from -1×10^{12} to $+1 \times 10^{12}$ cm⁻². The electrical response is evaluated at 50 K and 350 K, as presented in Fig. 14(a) and Fig. 14(b), respectively, with a drain-to-source voltage of 100 mV. The effect of interface trap charges on carrier transport is determined by the variation of the electrostatic potential at the

semiconductor–oxide interface, which in turn shifts channel formation and the threshold voltage (V_T).

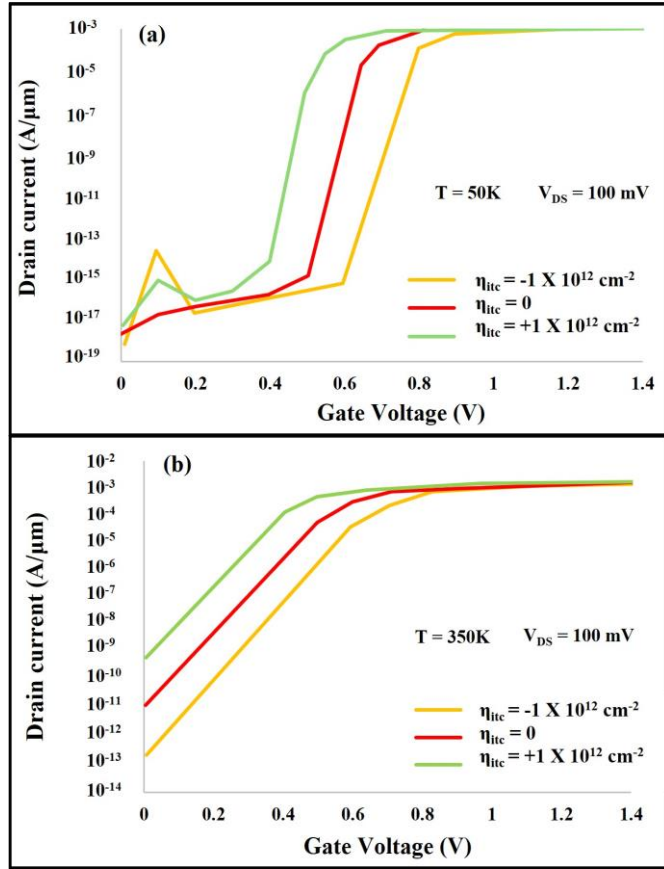


Figure 14: Transfer characteristics of the proposed DCT-DG-JL-MOSFET under different η_{itc} at (a) 50 K and (b) 350 K, demonstrating the influence of trap polarity on threshold voltage and I_D .

The dependence of the interface-trap polarity is clearly shown in the device operated at 50 K, as demonstrated in Fig. 14(a). For the negative-side interface traps ($\eta_{itc} = -1 \times 10^{12} \text{ cm}^{-2}$), the transfer curve shifts towards more positive V_g , indicating an increase in V_T and a decrease in I_D . This behavior arises from the formation of acceptor-like interface states that absorb free electrons, thereby reducing the number of free electrons available to conduct in the channel. Thus, a larger gate bias is required to form an inversion channel, leading to poorer electrostatic performance. The positively charged interface traps ($\eta_{itc} = +1 \times 10^{12} \text{ cm}^{-2}$) move the transfer characteristics towards the negative V_g . The introduction of donor-like interface states modifies the channel charge distribution, providing an easier path for channel charge transport, thereby increasing current conduction and decreasing the threshold voltage [35].

The same behavior is observed at 350 K, as shown in Fig. 14(b). But the impact of interface traps becomes comparatively less significant at higher OTs, leading to greater thermal carrier generation and making the device less sensitive to interface defects. Negative interface traps still cause a higher threshold voltage and lower I_D . In contrast, positive interface traps still contribute to increased current conduction, albeit to a smaller

extent at higher temperatures. In Fig. 14(a) and Fig. 14(b), the sensitivity of the proposed DCT-DG-JL-MOSFET to interface-trap charges increase with increasing depth of cryogenic operation. At lower temperatures, the reduced energy available restricts the creation of carriers, increasing the net reliance on interface states. Therefore, the polarity difference can become significant with moderate deviations in the trap value, leading to substantial shifts in the V_T and transfer characteristics. The results also show that negative interface traps degrade the electrical characteristics by reducing channel formation, while positive interface traps improve electron transport through the channel. Hence, it is vital for CMOS to achieve stable electrostatic characteristics and uniform switching performance in cryogenic applications such as quantum computing, to minimize interface traps during fabrication.

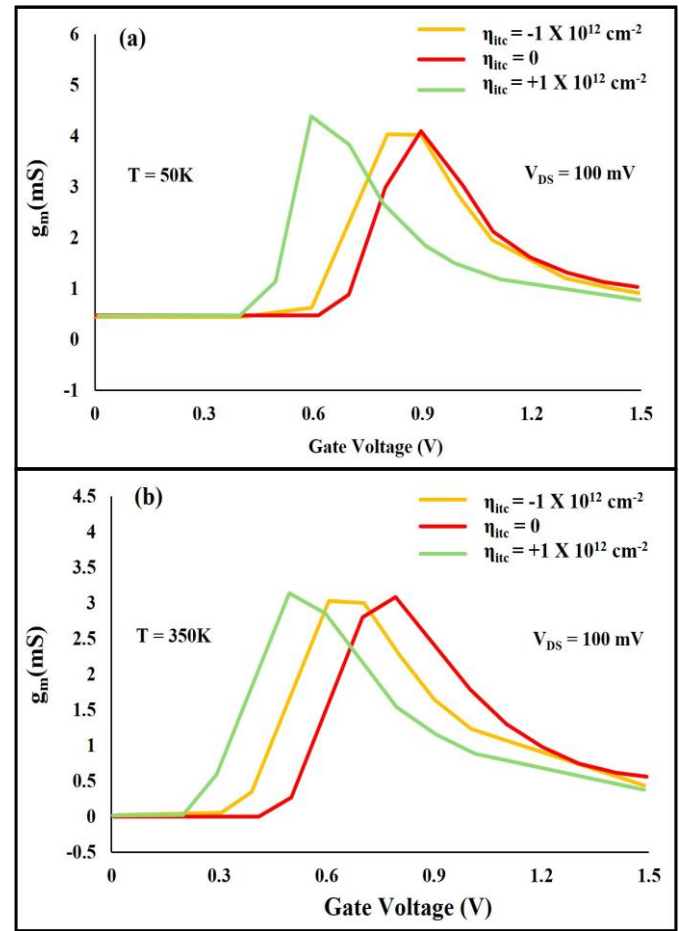


Figure 15: Effect of interface trap charge density on the g_m characteristics of the proposed DCT-DG-JL-MOSFET at (a) 50 K and (b) 350 K.

Fig. 15(a) and Fig. 15(b) show the g_m characteristics of the proposed DCT-DG-JL-MOSFET as a function of V_{DS} at 50 K and 350 K, respectively, for different values of η_{itc} . Three interface-trap conditions, $\eta_{itc} = -1 \times 10^{12}$, 0, and $\eta_{itc} = +1 \times 10^{12} \text{ cm}^{-2}$, are assessed to study the effect of the interface defect on the analog behavior. Note that, at both OTs, the transconductance grows with the V_g , peaks, and eventually decreases for a higher gate bias. This behavior is linked to the

progressive development of a channel that is then degraded in mobility because of the strengths.

The electrical polarity of the interfaces significantly affects the transconductance properties. The presence of positive interface trap charges shifts the gm peak towards lower V_g , reflecting improved channel formation and carrier transport. On the other hand, when the interface traps carry a negative charge, increasing the gate bias is necessary to reach the maximum transconductance, because an electron trapped at the semiconductor–oxide interface reduces the channel conductivity. The response of the trap-free device falls in between these two extremes. Additionally, the impact of interface traps is greater at 50 K than at 350 K, suggesting that these traps capture more carriers during cryogenic operation due to reduced thermal carrier generation. As the V_g increases, transconductance appears to decrease slowly for all trap configurations, as the vertical electric field increases and drives carriers into regions where surface roughness and interface scattering prevail. The scattering mechanisms reduce carrier mobility and, therefore, transconductance [36-38]. Results show that the interface trap charge density is an important reliability parameter that affects the analog performance at the DC operating conditions.

3.5 Transient Response at DCT

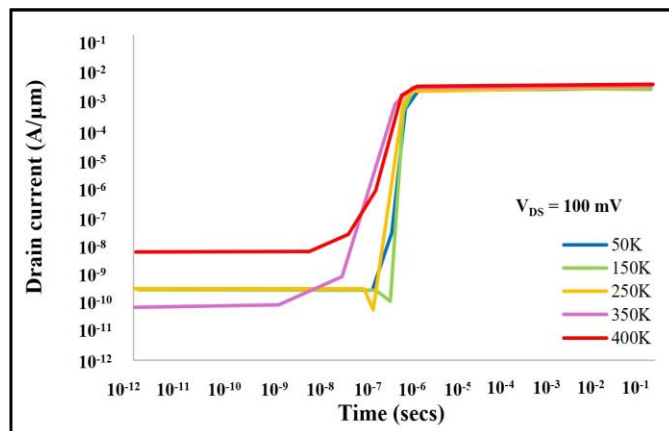


Figure 16: Transient drain-current response at different temperatures.

The transient response at different temperatures is shown in Fig. 16 for $V_{DS} = 100$ mV over the OT range of 50K to 400K. The transient analysis response was obtained using a V_g of 1.5 V, a transient time of 10^{-12} s, a ramp time of 10^{-6} s, and a stop time of 10^{-1} s to analyze the dynamic switching behavior of the device. The steady-state I_D is reached sooner as the OT decreases, indicating a shorter settling time and faster switching response. This improvement is mainly due to increased carrier mobility and reduced phonon scattering under DC conditions. The transient parameters observed under different temperature conditions confirm that the proposed DCT-DG-JL-MOSFET can be used effectively in high-speed, low-delay cryogenic CMOS circuits and in quantum computing applications. When the gas temperature decreases noticeably from 400K to 50K, the gas's settling time decreases. As shown in the figure, the device has a fast response time

during operation under DC conditions. As shown in the inset, the device can reach its operating condition in the shortest time under DC conditions. This suggests that the transistor's dynamic performance is improved at lower temperatures. The improved transient response is likely attributable to differences in carrier transport properties during operation at cryogenic temperatures. This reduces phonon scattering, thereby increasing carrier mobility and charge-channel transport by lowering the temperature. Furthermore, impurity freeze-out contributes to the electrostatic control, leading to quicker channel formation and current stabilization. This, in turn, means that the I_D can be switched instantaneously with the device's gate inputs, resulting in better switching and faster settling time. This decreased response time at low temperatures is particularly beneficial for high-speed electronic devices. The more quickly the settling of the current in the motor sets in, the less propagation delay will be, and the more responsive the circuit will be. These properties are key for advanced CMOS-based platforms for cryogenic applications, as well as for quantum interfaces, which are also application areas where the speed of signal processing and time control are essential. Hence, the transient analysis also shows that the proposed DCT-DG-JL-MOSFET exhibits good transient performance in DC conditions and can be a candidate for high-speed, low-delay quantum computational applications.

4. Conclusion

The behavior of high-k stacked DG junctionless MOSFETs has been thoroughly studied using a wide range of DC, analog, RF, reliability, and transient analyses at deep DCTs. The study shows that it is possible to achieve a substantial change in the device's electrostatic behavior by decreasing its OT. Suppression of phonon scattering and impurity freeze-out effects at cryogenic temperatures provides greater improvements in carrier transport, thereby enhancing device performance across various operating domains. The DC analysis showed that better switching properties were obtained at lower temperatures, due to lower leakage current, a higher I_{ON}/I_{OFF} current ratio, and better subthreshold properties. These enhancements suggest that channel control is more electrostatic in nature and that these devices are better suited for low-power electronic applications. Furthermore, it is shown that the Analog performance evaluation improves with transconductance, and that the improvement in energy efficiency in analog circuit design is understood, confirming the feasibility of the proposed structure for energy-efficient analog circuits at cryogenic temperatures. RF characteristics were good, with a higher cut-off frequency. A stable operation frequency-range stability accompanied by UPG/GBP. The parasitic-effect reduction and carrier-mobility improvement were observed to be responsible for the improvement in RF performance. Furthermore, the Stern stability analysis showed that the device is stable and reliable in a DC environment, making it a potential candidate for higher-level RF and mixed-signal applications. This reliability study was also confirmed by analysing the influence of measurement η_{itc} at the semiconductor–dielectric interface. From the results, it can be seen that the negative interface traps should be avoided to

improve the electrostatic properties by enhancing current conduction and transconductance. The electrostatic properties, on the other hand, are not affected when holes are trapped inside the oxide at the interface. With holes trapped inside the oxide at the interface, the electrostatic properties, on the other hand, are not affected. The observations demonstrate the impact of interface quality on device reliability, particularly at low temperatures. Lastly, according to transient analysis, a reduction in temperature led to a shorter settling time, resulting in a quicker switching response and a smaller operating delay. Overall, the proposed DCT-DG-JL-MOSFET provides very good electrostatic control, superior analog and RF properties, enables more stable operation, and exhibits excellent dynamic response at cryogenic temperatures. It has some very promising properties for low-power Cryogenic CMOS platforms, high-performance quantum computing systems, and even superconducting devices.

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